REMARKS

A new proposed FIG. 1 is submitted herewith in response to the objection to FIG. 1.

The rejection of claims 1-19 under 35 USC §112 is respectfully traversed because the basis for the rejection is apparently a typographical error. Specifically, claim 1 part (e) should have referenced "steps (f) - (g)" instead of "steps (f) - (h)" as originally filed. One skilled in the art would have understood from the formatting and content of originally filed claim 1 that the reference to "(h)" should have been "(g)". Therefore, the claim is amended to correct a typographical error and not for the purpose of patentability.

The allowability of claims 6-12 and 19 is acknowledged. However, no amendment is made because the base claims are also thought to be allowable over the cited art.

The Office Action does not establish that claims 1-5, 13-18, and 20 are unpatentable under 35 USC §103(a) over US patent 6,216,257 to Agrawal et al. (hereinafter "Agrawal") in view of US patent 6,631,508 to Williams (hereinafter "Williams"). The rejection is respectfully traversed because the Office Action fails to show that all the limitations are suggested by the references, fails to provide a proper motivation for modifying the teachings of Agrawal with teachings of Williams, and fails to show that the combination could be made with a reasonable likelihood of success.

The Office Action does not establish that the combination teaches the claimed invention of a method for simulating a circuit design for a programmable logic device (PLD). The limitations not shown to be taught by the combination include: (a) reading a configuration bitstream; (b) constructing objects in a computer memory, each object corresponding to a configurable element of the PLD as configured in the configuration bitstream, and each object having associated therewith an output signal state and one or more input signal states; (c) generating events in response to signal values in the configuration bitstream, each event including an object

identifier, an input signal identifier, and an input signal state; (d) for each event, updating the output signal state and an input signal state of a corresponding object in response to the input signal state of the event and type of configurable element; (e) performing steps (f) - (g) if processing an event changes the output signal state of an object; (f) finding the configurable elements that are connected to the output signal; and (g) generating events for the objects corresponding to the configurable elements from step (f).

As explained below, neither Agrawal nor Williams teach or suggest these limitations. The claims clearly demonstrate that a simulation model (the "objects" and "events") is constructed in reverse of prior simulation flows. That is, the simulation model is constructed from a configuration bitstream, not from a high-level design.

The cited section of Agrawal neither shows nor suggests reading a configuration bitstream and constructing the objects for simulation from the bitstream. The cited section at col. 3, ll. 49-55 teaches generating configuration instruction signals that will be supplied to an un-programmed FPGA to implement a design. The cited section at col. 8, ll. 40-44 teaches that Boolean functions may be implemented with FPGA lookup tables, and the Boolean functions are described in VHDL (col. 8, ll. 19-28). Thus, it is clear that Agrawal does not read a bitstream and from the bitstream generate the objects used in simulation.

The Office Action mistakenly alleges that Williams teaches (c) generating events in response to signal values in the configuration bitstream, each event including an object identifier, an input signal identifier, and an input signal state; and (d) for each event, updating the output signal state and an input signal state of a corresponding object in response to the input signal state of the event and type of configurable element. Williams describes approaches for placing a circuit design, not methods for simulating. Thus, it is not understood how the cited teachings of Williams could be reasonably construed to suggest the claimed generating and processing of

events. For example, Williams' column 9 shows example VHDL placement directives, and column 10 describes specific placement directive commands used on placing parts of the design. Those skilled in the art will recognize that placement directives are very different from simulation events.

The alleged motivation for combining Williams with Agrawal is improper. The alleged motivation states that "it would have been obvious … to modify mapping VHDL constructs to the fine and/or coarse grain resources of the targeted FPGA device/family as taught in Agrawal with the steps as disclosed in Williams since the mapping step involves mapping the netlist to particular configurable resources of the device as taught in Williams." The alleged motivation is improper because it fails to provide any evidence that Agrawal's approach for mapping is in any way deficient, fails to provide any evidence to indicate what improvement Williams' teachings might offer, and even fails to provide evidence of how teachings of Agrawal's might be modified to accommodate Williams' approach. It is not apparent how Agrawal's method could be modified with teachings of Williams. Therefore, the alleged motivation is improper.

Claims 2-5 and 13-18 contain further limitations that further detail the limitations of claim 1. Therefore, *prima facie* obviousness is not established for at least the reasons set for the above in regards to the rejection of claim 1.

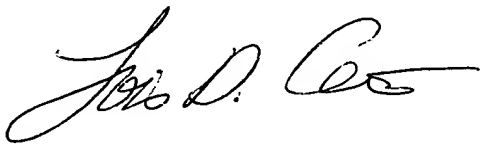
Claim 20 is an apparatus claim. To the extent that the limitations of claim 20 are similar to those of claim 1, *prima facie* obviousness is not established for claim 20 for at least the reasons set forth above for claim 1.

The rejection of claims 1-5, 13-18, and 20 over the Agrawal-Williams combination should be withdrawn because the Office Action fails to show all the limitations are suggested by the combination, fails to provide a proper motivation for combining the references, and fails to show that the combination could be made with a reasonable likelihood of success.

CONCLUSION

Reconsideration and a notice of allowance are respectfully requested in view of the Remarks presented above. If the Examiner has any questions or concerns, a telephone call to the undersigned is invited.

Respectfully submitted,



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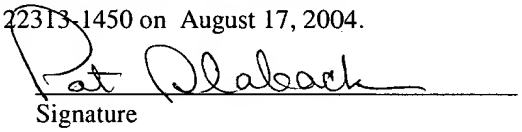
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